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LAST FRAME REPEAT

RELATED APPLICATIONS

[001] [Not Applicable]

FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT

[002] [Not Applicable]

[MICROFICHE/COPYRIGHT REFERENCE]

[003] [Not Applicable]

BACKGROUND OF THE INVENTION

[004] A display device usually receives video frames from another device that is attached to, but was manufactured separately from the display device. The device providing the frames and the display device are synchronized by means of a vertical synchronization pulses Vsynch and horizontal synchronization pulses Hsynch. The display device signifies the beginning of a time period for the display of a frame by transmitting a vertical synchronization pulse (Vsynch).

[005] Between the vertical synchronization pulse and the first horizontal synchronization pulse, there is a period of time known as the vertical blanking interval VBI. During the VBI, preparations are made for displaying the next frame. The preparation can include receiving information regarding the next frame for display and an

address in a buffer storing the first pixel of the next frame for display.

[006] Ideally, the foregoing information is received before or during the VBI. However, if the foregoing is not received, the device providing the frames may not be able to provide the next frame for display. The foregoing can potentially result in a noticeable degradation of quality in the display of the video.

[007] Further limitations and disadvantages of conventional and traditional approaches will become apparent to one of skill in the art, through comparison of such systems with embodiments presented in the remainder of the present application with references to the drawings.

BRIEF SUMMARY OF THE INVENTION

[008] Described herein is a system and method for repeating a last frame.

[009] In one embodiment, there is presented a method for displaying frames. The method comprises providing a first frame, waiting to receive information about a second frame to display, after displaying the first frame, and providing the first frame, if the information regarding the second frame is not received before a predetermined time.

[0010] In another embodiment, there is presented a system for displaying frames. The system comprises a display engine, and a host processor. The display engine provides a first frame. The host processor provides information about a second frame to the display engine, after the display engine provides the first frame. The display engine provides the first frame, if the host processor does not provide the information regarding the second frame to the display engine before a predetermined time.

[0011] In another embodiment, there is presented a feeder for providing a frame. The feeder comprises a first one or more registers, a circuit, and a host processor. The first one or more registers stores one or more starting address for a first frame. The circuit calculates starting addresses for one or more rows of the first frame following a vertical synchronization pulse associated with the first frame. The host processor writes one or more starting address for a second frame to the first one or more registers. The first one or more registers stores the one or more starting address for the first frame until the host

processor writes the one or more starting address for the second frame to the first one or more registers.

[0012] These and other advantages and novel features of the present invention, as well as details of an illustrated embodiment thereof, will be more fully understood from the following description and drawings.

BRIEF DESCRIPTION OF SEVERAL VIEWS OF THE DRAWINGS

[0013] **FIGURE 1** is a block diagram describing an exemplary display timing diagram;

[0014] **FIGURE 2** is a flow chart for displaying a frame in accordance with an embodiment of the present invention;

[0015] **FIGURE 3** is a block diagram of a decoder system in accordance with an embodiment of the present invention;

[0016] **FIGURE 4** is a block diagram of a display engine in accordance with an embodiment of the present invention; and

[0017] **FIGURE 5** is a block diagram of an exemplary feeder in accordance with an embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0018] Referring now to **FIGURE 1**, there is illustrated a block diagram describing a display timing diagram. Video data comprises a series of consecutive frames 100. Each frame 100 is associated with a particular time interval. A display device displays the frames at the specific predetermined time with highly synchronized timing.

[0019] The frames 100 further comprise any number of lines 0...N of pixels. The display device displays the lines 0...N at a particular time interval within the time interval for displaying the frame. In the case of a progressive display, the lines 0...N are displayed in consecutive order, line 0, line 1, line 2,...line N.

[0020] The display device usually receives the frames from another device that is attached to, but was manufactured separately from the display device. The device providing the frames and the display device are synchronized by means of a vertical synchronization pulses Vsynch and horizontal synchronization pulses Hsynch. The display device signifies the beginning of a time period for the display of a frame by transmitting a vertical synchronization pulse (Vsynch). The display device signifies the time period for displaying a new line in a frame 100(x) by transmitting a horizontal synchronization pulse Hsynch. The device providing the frames uses the foregoing vertical/horizontal synchronization pulses to follow the timing of the display device, and provides the appropriate line 100(x) of the appropriate frame 100 for display at the appropriate time.

[0021] For a progressive display, each vertical synchronization pulse Vsynch is followed by horizontal synchronization pulses $Hsynch_0$, $Hsynch_1$, $Hsynch_2$,... $Hsynch_N$, associated with each line 100(0), 100(1), 100(2),...100(N) in the frame 100. Responsive to the horizontal synchronization pulses $Hsynch_x$, the display device receives and displays the horizontal line 100(x) associated with the horizontal synchronization pulse.

[0022] Between each consecutive Hsynch, there is a time period to allow for preparation to display the next line. The preparations can include, for example, determining a memory address in a buffer that stores the pixels of the next line.

[0023] Additionally, between the vertical synchronization pulse Vsynch and the first horizontal synchronization pulse $Hsynch_0$, there is a period of time known as the vertical blanking interval VBI. During the VBI preparations are made for displaying the next frame. The preparation can include receiving information regarding the next frame for display and an address in a buffer storing the first pixel of the next frame for display.

[0024] Ideally, the foregoing information is received before or during the VBI. However, if the foregoing is not received, the device providing the frames may not be able to provide the next frame for display. The foregoing can potentially result in a noticeable degradation of quality in the display of the video. To reduce the degradation in the quality of the display of the video caused by the foregoing, where the device does not receive the information regarding the next frame, e.g., 100_1 for display by a predetermined time, such as the first $Hsynch_0$ following $Vsynch_1$, the device provides the previous frame 100_0 for

display during the display time (the time period between $Vsynch_1$ and the following Vsynch) for frame 100_1.

[0025] Referring now to **FIGURE 2**, there is illustrated a flow diagram for displaying frames in accordance with an embodiment of the present invention. At 205, the device for providing frames for display to the display device receives information regarding the first frame for display and provides the first frame for display. After providing the first frame for display, the device waits (210) to receive information regarding the next frame for display. At 215, if the device receives the information before the predetermined time, the device provides (220) the next frame for display. If at 215, the device does not receive the information before the predetermined time, the device provides (225) the frame provided during 205 for display again.

[0026] Referring now to **FIGURE 3**, there is illustrated a block diagram describing an exemplary decoder system for providing frames for display to a display device in accordance with an embodiment of the present invention. A processor, that may include a CPU 90, reads transport bitstream 65 into a transport bitstream buffer 32 within an SDRAM 30.

[0027] The data is output from the transport bitstream buffer 32 and is then passed to a data transport processor 35. The data transport processor 35 then demultiplexes the transport bitstream 65 into constituent transport bitstreams. The constituent packetized elementary bitstream can include for example, video transport bitstreams, and audio transport bitstreams. The data transport processor 35 passes an audio transport bitstream to an audio decoder 60 and a video transport bitstream to a video transport

processor 40.

[0028] The video transport processor 40 converts the video transport bitstream into a video elementary bitstream and provides the video elementary bitstream to a video decoder 45. The video decoder 45 decodes the video elementary bitstream, resulting in a sequence of decoded video frames. The decoding can include decompressing the video elementary bitstream. The decoded video data includes a series of frames. The frames are stored in a frame buffer 48.

[0029] The display engine 50 is responsible for providing a bitstream to a display device, such as a monitor or a television. The display device and the decoder system are synchronized by horizontal and vertical synchronization pulses. Between the vertical synchronization pulse Vsynch and the first horizontal synchronization pulse $Hsynch_0$, there is a period of time known as the vertical blanking interval VBI. During the VBI, preparations are made for displaying the next frame. The preparation can include the host processor 90 determining the frame for display and providing an address in the frame buffer storing the first pixel of the frame for display to the display engine 50.

[0030] Ideally, the display engine 50 receives foregoing information before or during the VBI. However, if the foregoing is not received, the display engine 50 may not be able to provide the next frame, frame 100_1, for display. The foregoing can potentially result in a noticeable degradation of quality in the display of the video. To reduce the degradation in the quality of the display of the video caused by the foregoing, where the display engine 50 does not receive the information regarding the next frame,

e.g., 100_1 for display by a predetermined time, such as the first $Hsynch_0$ following $Vsynch_1$, the display engine 50 provides the previous frame 100_0 for display during the display time (the time period between $Vsynch_1$ and the following Vsynch) for frame 100_1.

[0031] Referring now to **FIGURE 4**, there is illustrated a block diagram of the display engine 50 in accordance with an embodiment of the present invention. The display engine 50 includes a scalar 705, a compositor 710, a feeder 715, and a deinterlacing filter 720. The feeder 715 rasterizes the pixels of the displayed frame.

[0032] The feeder 715 and the display device are synchronized by horizontal and vertical synchronization pulses. During the VBI, preparations are made for displaying the next frame. The preparations can include the host processor 90 determining the frame for display and providing an address in the frame buffer storing the first pixel of the frame for display to the feeder 715.

[0033] Ideally, the feeder 715 receives foregoing information before or during the VBI. However, if the foregoing is not received, the feeder 715 may not be able to rasterize and provide the next frame, frame 100_1, for display. The foregoing can potentially result in a noticeable degradation of quality in the display of the video. To reduce the degradation in the quality of the display of the video caused by the foregoing, where the pixel feeder 715 does not receive the information regarding the next frame, e.g., 100_1 for display by a predetermined time, such as the first $Hsynch_0$ following $Vsynch_1$, the pixel feeder 715 rasterizes and provides the previous frame 100_0 for display during the display time (the time period between $Vsynch_1$ and the following Vsynch) for frame 100_1.

[0034] Referring now to **FIGURE 5**, there is illustrated a block diagram of the feeder 715 in accordance with an embodiment of the present invention. The feeder 715 comprises an RBUS interface 805, a line address computer (LAC) 810, a Burst Request Manager (BRM) 815, an input data write unit (IDWU) 820, a buffer 840, a pixel feeder 835, a BVB protocol generator 825, and an output buffer 830.

[0035] The host processor 90 programs the feeder 715 during the VBI with the addresses in the frame buffer 48 storing the starting chroma and luma pixels of the frame. The starting addresses are provided to the feeder 715 via a luma starting address register 805Y and a chroma starting address register 805C in the RBUS interface 805. After providing the parameters to the RBUS interface 805, the host 90 sets a start parameter in the RBUS interface 805.

[0036] The feeder 715 fetches each pixel line in a series of bursts and stores the pixels in the buffer 840. The initial starting luma and chroma addresses are provided to the BRM 815. When the BRM 815 receives the starting luma and chroma addresses, the start parameter in the RBUS Interface 805 is deasserted.

[0037] The BRM 815 issues the commands for fetching the luma and chroma pixels in the first line of the frame/field. The IDWU 820 effectuates the commands. The pixel feeder 835 retrieves the pixels from the buffer 840, and outputs a rasterized stream formatted in accordance with the display format. The output rasterized stream is provided to the output buffer, via the BVB protocol generator.

[0038] After the BRM 815 receives the starting addresses of the frame, the LAC 810 detects deassertion of the start parameter and calculates the starting address of the next

line and stores the addresses in the RBUS Interface 805 and reasserts the start parameter. The starting addresses of the next line are determined by appropriately incrementing the starting address of the current line.

[0039] The LAC 810 includes a last luma line start register 810Y and a last chroma line start register 810C. Initially, the address write to the registers 805Y and 805C are transferred to the registers 810Y and 810C. The LAC 810 calculates the starting addresses for a line 100(x) by incrementing the registers 810Y and 810C. The registers 810Y, 810C then store the starting address for the line 100(x). To calculate the starting addresses for a line 100(x+1), the LAC 810 increments the registers 810Y and 810C.

[0040] When the BRM 815 and IDWU 820 finish transferring the current line to the buffer 840, the BRM 815 receives the starting addresses for the next line from the RBUS Interface 805. When the BRM 815 receives the starting addresses for the next line, the start parameter is deasserted. The foregoing process is repeated until the end of the picture.

[0041] The operation of the LAC 810 is described in greater detail in 60/495,695, that is incorporated herein by reference.

[0042] The RBUS Interface 805 is programmed with the starting addresses of the previous frame 100_0 following the previous Vsynch, $Vsynch_0$, in registers 805Y, 805C. Ideally, the RBUS Interface 805 receives starting addresses of frame 100_1 in registers 805Y, 805C before or during the VBI following $Vsynch_1$. Where the RBUS Interface 805 receives the starting addresses of frame 100_1 prior to a predetermined time, such as $Hsynch_0$ following $Vsynch_1$, the starting

addresses of frame 100_1 overwrite the starting addresses of frame 100_0.

[0043] If the addresses are not received, the feeder 715 may not be able to rasterize and provide the next frame, frame 100_1, for display. The foregoing can potentially result in a noticeable degradation of quality in the display of the video. However, the RBUS interface 805 maintains the starting addresses for the previous frame 100_0. To reduce the degradation in the quality of the display of the video caused by the foregoing, where the RBUS interface 805 does not receive the starting addresses for the next frame, e.g., 100_1 for display by a predetermined time, such as the first $Hsynch_0$ following $Vsynch_1$, the pixel feeder 715 rasterizes and provides the previous frame 100_0 for display during the display time (the time period between $Vsynch_1$ and the following Vsynch) for frame 100_1. The feeder 715 rasterized the previous frame 100_0 based on the starting addresses programmed into the registers 805Y, 805C following $Vsynch_0$.

[0044] One embodiment of the present invention may be implemented as a board level product, as a single chip, application specific integrated circuit (ASIC), or with varying levels integrated on a single chip with other portions of the system as separate components. The degree of integration of the system will primarily be determined by speed and cost considerations. Because of the sophisticated nature of modern processors, it is possible to utilize a commercially available processor, which may be implemented external to an ASIC implementation of the present system. Alternatively, if the processor is available as an ASIC core or logic block, then the commercially available processor can be implemented as part

of an ASIC device with various functions implemented as firmware.

[0045] While the invention has been described with reference to certain embodiments, it will be understood by those skilled in the art that various changes may be made and equivalents may be substituted without departing from the scope of the invention. In addition, many modifications may be made to adapt particular situation or material to the teachings of the invention without departing from its scope. Therefore, it is intended that the invention not be limited to the particular embodiment(s) disclosed, but that the invention will include all embodiments falling within the scope of the appended claims.